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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/700,464	11/15/2000	Terunao Hanaoka	107284	5910

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EXAMINER
ANDUJAR, LEONARDO

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 09/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/700,464	HANAOKA ET AL.	
	Examiner	Art Unit	
	Leonardo Andújar	2826	

-- Th MAILING DATE of this communication appears on the cover she t with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 June 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17 and 19-36* is/are pending in the application.

4a) Of the above claim(s) *25-36* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17 and 19-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 05/27/2003 has been entered.

Election/Restrictions

2. Claims 25-36 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected invention, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in Paper No. 4.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein

were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1-17, 19 and 21–24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Greer (US 5,470,787) in view of Elenius et al. (US 6,441,487).

6. Regarding claim 1, Greer (e.g. fig. 5) shows a semiconductor device comprising:

- A semiconductor element 24 having a plurality of electrodes 22;
- An interconnect pattern (36, 38, 40) electrically connected to the electrodes;
- And external terminals 42 electrically connected to the interconnect pattern.

7. Greer shows a plurality of insulating or passivation layers (26, 28 and 30) formed around the external terminals on the interconnect pattern. As shown in figure 5, each of the insulating layers has a hole that includes an opening portion. The external terminals are positioned in the opening portions that have one-step portion formed on the inside surface. Greer, however, shows that external terminals overlap the electrodes. Elenius (e.g. figs. 1 and 2) shows a semiconductor device including a semiconductor element 14 having external terminals 28 electrically connected to a interconnect pattern 30 without overlapping electrodes 18. According to Elenius this type of embodiment provides an improved chip scale package that has a small form factor, i.e. the resulting chip scale package is not larger than the size of the original integrated circuit (col. 3/lls. 16-41). Elenius discloses that the size and the amount of the solder bumps are

compromised due to the fact that the solder pads are typically located at the perimeter of the integrated circuit. Elenius discloses that the solder bump contact pads can be redistributed internally, away form the outer perimeter of the integrated circuit; the size of such solder bumps is unchanged. Therefore, the requirements of complex integrated circuits can be fulfilled (col. 2/lls. 25-40). It would have been obvious to one of ordinary skill in the art at the time the invention was made to electrically connect the interconnect the patterns and the external terminals disclosed by Greer without overlapping the electrodes in order to provide an improved chip scale package having a small form factor, i.e. the resulting chip scale package is not larger than the size of the original integrated circuit, and to internally redistribute the solder bump contact pads, away form the outer perimeter of the integrated circuit, in order to fulfill the requirements of complex integrated circuit as taught by as taught by Elenius.

8. Regarding claim 2, Greer in view of Elenius shows a plurality of insulating layers. In reference to the claim language referring to stress relieving function, intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. In re Casey, 152 USPQ 235 (CCPA 1967); In re Otto, 136 USPQ 458, 459 (CCPA 1963).

9. Regarding claim 3, Greer shows that the insulating layer 30 can be made of polyimide (col. 8/lls. 25-26).

10. Regarding claim 4, Greer shows that the insulating layers contact the external terminals at opening portions each of which has an inclined surface providing a taper increasing in size form a lower layer to higher layer of the insulating layers.

11. Regarding claim 5, Greer shows that each of the external terminals includes a base and a connection portion provide on the base. Also, the base is provided in an opening portion through which each of the external terminals contact the insulating layers.

12. Regarding claim 6, Greer shows that the insulating layers contact the external terminals at opening portions each of which is formed with a curved surface.

13. Regarding claim 7, Greer in view of Elenius shows that the interconnect pattern is formed on the layer 16 which is below the plurality of insulating layers. In reference to the claim language referring to stress relieving function, intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. In re Casey, 152 USPQ 235 (CCPA 1967); In re Otto, 136 USPQ 458, 459 (CCPA 1963).

14. Regarding claim 8, Greer shows that the uppermost layer of the insulating layers is formed over the whole surface of the second layer of the insulating layers from the uppermost layer except for an area of the external terminal.

15. Regarding claim 9, Greer shows that the uppermost layer 30 of the insulating layers has an area smaller that an area of the second layer 28 of the insulating layers forms the uppermost layer.

16. Regarding claim 10, Greer shows a plurality of insulating or passivation layers (26, 28 and 30) formed around the external terminals on the interconnect pattern. The insulating layers include an upper layer 30 and a lower layer of different characteristics (i.e. layer thickness).

17. Regarding claim 13, Greer (e.g. fig. 5) shows a semiconductor device comprising:

- A semiconductor element 24 having a plurality of electrodes 22;
- An interconnect pattern (36, 38, 40) electrically connected to the electrodes;
- And external terminals 42 electrically connected to the interconnect pattern.

18. Also, Greer shows that the interconnect pattern is formed on an insulating layer that has protrusions and depressions. The external terminals are formed in the depressions. Greer, however, shows that external terminals overlap the electrodes. Elenius (e.g. figs. 1 and 2) shows a semiconductor device including a semiconductor element 14 having external terminals 28 electrically connected to a interconnect pattern 30 without overlapping electrodes 18. According to Elenius this type of embodiment provides an improved chip scale package that has a small form factor, i.e. the resulting chip scale package is not larger than the size of the original integrated circuit (col. 3/lls. 16-41). Elenius discloses that the size and the amount of the solder bumps are compromised due to the fact that the solder pads are typically located at the perimeter

of the integrated circuit. Elenius discloses that the solder bump contact pads can be redistributed internally, away form the outer perimeter of the integrated circuit; the size of such solder bumps is unchanged. Therefore, the requirements of complex integrated circuits can be fulfilled (col. 2/lls. 25-40). It would have been obvious to one of ordinary skill in the art at the time the invention was made to electrically connect the interconnect the patterns and the external terminals disclosed by Greer without overlapping the electrodes in order to provide an improved chip scale package having a small form factor, i.e. the resulting chip scale package is not larger than the size of the original integrated circuit, and to internally redistribute the solder bump contact pads, away form the outer perimeter of the integrated circuit, in order to fulfill the requirements of complex integrated circuit as taught by as taught by Elenius.

19. Regarding claim 14, Greer in view of Elenius shows a plurality of insulating layers. In reference to the claim language referring to stress relieving function, intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. In re Casey, 152 USPQ 235 (CCPA 1967); In re Otto, 136 USPQ 458, 459 (CCPA 1963).

20. Regarding 15, Elenius teaches that the passivation and /or insulating layer is formed of polyimide (col. 6/lls. 31-56).

21. Regarding claim 16, Greer shows that the external terminals includes a base and a connection portion provided on the base. The base and the interconnect pattern are constructed as a single member.

22. Regarding claim 17, Greer shows that the depressions are formed to have an opening extremity lager than the bottom.

23. Regarding claims 11, 12 and 19, Greer in view of Elenius teaches that the passivation or insulating layer can be made form different resins (col. 6/lls.31-56). Different materials have different physical properties such as thermal expansion coefficient, density, and Young's modulus. Therefore, Greer in view of Elenius suggested that the coefficient of thermal expansion of the upper layer is greater that the thermal expansion coefficient of the lower layer. Also, the Young's modulus of the lower layer is greater than the Young's modulus of the upper layer. Note that the terms lower and upper are relative terms that can arbitrary selected. For example, the layer 26 can be recognized as lower layer if the direction increment is arbitrary selected from substrate to the external surface of 30. However, same layer can be recognized as the upper layer if the direction increment is arbitrary selected from surface of the layer 30 to the substrate. Furthermore, the insulating layers the upper layer 30 and the lower layer have different characteristics (i.e. layer thickness).

24. Regarding claim 21, Greer that a semiconductor device is mounted in a circuit board (col. 1/lls. 19-29). Also, Greer (e.g. fig. 5) shows that the semiconductor device comprises:

- A semiconductor element 24 having a plurality of electrodes 22;

- An interconnect pattern (36, 38, 40) electrically connected to the electrodes;
- And external terminals 42 electrically connected to the interconnect pattern.

25. Greer shows a plurality of insulating or passivation layers (26, 28 and 30) formed around the external terminals on the interconnect pattern. As shown in figure 5, each of the insulating layers has a hole that includes an opening portion. The external terminals are positioned in the opening portions that have one-step portion formed on the inside surface. Greer, however, shows that external terminals overlap the electrodes. Elenius (e.g. figs. 1 and 2) shows a semiconductor device including a semiconductor element 14 having external terminals 28 electrically connected to a interconnect pattern 30 without overlapping electrodes 18. According to Elenius this type of embodiment provides an improved chip scale package that has a small form factor, i.e. the resulting chip scale package is not larger than the size of the original integrated circuit (col. 3/lls. 16-41). Elenius discloses that the size and the amount of the solder bumps are compromised due to the fact that the solder pads are typically located at the perimeter of the integrated circuit. Elenius discloses that the solder bump contact pads can be redistributed internally, away form the outer perimeter of the integrated circuit; the size of such solder bumps is unchanged. Therefore, the requirements of complex integrated circuits can be fulfilled (col. 2/lls. 25-40). It would have been obvious to one of ordinary skill in the art at the time the invention was made to electrically connect the interconnect the patterns and the external terminals disclosed by Greer without overlapping the electrodes in order to provide an improved chip scale package having a small form factor, i.e. the resulting chip scale package is not larger than the size of the original

integrated circuit, and to internally redistribute the solder bump contact pads, away form the outer perimeter of the integrated circuit, in order to fulfill the requirements of complex integrated circuit as taught by as taught by Elenius.

26. Regarding claim 22, Greer that a semiconductor device is mounted in a circuit board (col. 1/lls. 19-29). Also, Greer (e.g. fig. 5) shows that the semiconductor device comprises:

- A semiconductor element 24 having a plurality of electrodes 22;
- An interconnect pattern (36, 38, 40) electrically connected to the electrodes;
- And external terminals 42 electrically connected to the interconnect pattern.

27. Also, Greer shows that the interconnect pattern is formed on an insulating layer that has protrusions and depressions. The external terminals are formed in the depressions. Greer, however, shows that external terminals overlap the electrodes. Elenius (e.g. figs. 1 and 2) shows a semiconductor device including a semiconductor element 14 having external terminals 28 electrically connected to a interconnect pattern 30 without overlapping electrodes 18. According to Elenius this type of embodiment provides an improved chip scale package that has a small form factor, i.e. the resulting chip scale package is not larger than the size of the original integrated circuit (col. 3/lls. 16-41). Elenius discloses that the size and the amount of the solder bumps are compromised due to the fact that the solder pads are typically located at the perimeter of the integrated circuit. Elenius discloses that the solder bump contact pads can be redistributed internally, away form the outer perimeter of the integrated circuit; the size of such solder bumps is unchanged. Therefore, the requirements of complex integrated

circuits can be fulfilled (col. 2/lls. 25-40). It would have been obvious to one of ordinary skill in the art at the time the invention was made to electrically connect the interconnect the patterns and the external terminals disclosed by Greer without overlapping the electrodes in order to provide an improved chip scale package having a small form factor, i.e. the resulting chip scale package is not larger than the size of the original integrated circuit, and to internally redistribute the solder bump contact pads, away form the outer perimeter of the integrated circuit, in order to fulfill the requirements of complex integrated circuit as taught by as taught by Elenius.

28. Regarding claim 23, Greer (e.g. fig. 5) shows an electronic instrument having semiconductor device comprising:

- A semiconductor element 24 having a plurality of electrodes 22;
- An interconnect pattern (36, 38, 40) electrically connected to the electrodes;
- And external terminals 42 electrically connected to the interconnect pattern.

29. Greer shows a plurality of insulating or passivation layers (26, 28 and 30) formed around the external terminals on the interconnect pattern. Greer, however, shows that external terminals overlap the electrodes. Elenius (e.g. figs. 1 and 2) shows a semiconductor device including a semiconductor element 14 having external terminals 28 electrically connected to a interconnect pattern 30 without overlapping electrodes 18. According to Elenius this type of embodiment provides an improved chip scale package that has a small form factor, i.e. the resulting chip scale package is not larger than the size of the original integrated circuit (col. 3/lls. 16-41). Elenius discloses that the size and the amount of the solder bumps are compromised due to the fact that the solder

pads are typically located at the perimeter of the integrated circuit. Elenius discloses that the solder bump contact pads can be redistributed internally, away form the outer perimeter of the integrated circuit; the size of such solder bumps is unchanged. Therefore, the requirements of complex integrated circuits can be fulfilled (col. 2/lls. 25-40). It would have been obvious to one of ordinary skill in the art at the time the invention was made to electrically connect the interconnect the patterns and the external terminals disclosed by Greer without overlapping the electrodes in order to provide an improved chip scale package having a small form factor, i.e. the resulting chip scale package is not larger than the size of the original integrated circuit, and to internally redistribute the solder bump contact pads, away form the outer perimeter of the integrated circuit, in order to fulfill the requirements of complex integrated circuit as taught by as taught by Elenius.

30. Regarding claim 24, Greer (e.g. fig. 5) shows an electronic instrument having a semiconductor device comprising:

- A semiconductor element 24 having a plurality of electrodes 22;
- An interconnect pattern (36, 38, 40) electrically connected to the electrodes;
- And external terminals 42 electrically connected to the interconnect pattern.

31. Also, Greer shows that the interconnect pattern is formed on an insulating layer that has protrusions and depressions. The external terminals are formed in the depressions. Greer, however, shows that external terminals overlap the electrodes. Elenius (e.g. figs. 1 and 2) shows a semiconductor device including a semiconductor element 14 having external terminals 28 electrically connected to a interconnect pattern

30 without overlapping electrodes 18. According to Elenius this type of embodiment provides an improved chip scale package that has a small form factor, i.e. the resulting chip scale package is not larger than the size of the original integrated circuit (col. 3/lls. 16-41). Elenius discloses that the size and the amount of the solder bumps are compromised due to the fact that the solder pads are typically located at the perimeter of the integrated circuit. Elenius discloses that the solder bump contact pads can be redistributed internally, away form the outer perimeter of the integrated circuit; the size of such solder bumps is unchanged. Therefore, the requirements of complex integrated circuits can be fulfilled (col. 2/lls. 25-40). It would have been obvious to one of ordinary skill in the art at the time the invention was made to electrically connect the interconnect the patterns and the external terminals disclosed by Greer without overlapping the electrodes in order to provide an improved chip scale package having a small form factor, i.e. the resulting chip scale package is not larger than the size of the original integrated circuit, and to internally redistribute the solder bump contact pads, away form the outer perimeter of the integrated circuit, in order to fulfill the requirements of complex integrated circuit as taught by as taught by Elenius.

32. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Greer (US 5,470,787) in view of Elenius et al. (US 6,441,487) further in view of Kitayama et al. (US 5744382).

33. Regarding claim 20, Greer in view of Elenius shows most aspects of the instant invention (see comments above). However, Greer in view of Elenius does not disclose a protective film formed on the uppermost layer of the semiconductor device. Kitayama

(e.g. fig. 7) shows a semiconductor device having a protective film 4 formed on its uppermost layer. Also, Kitayama discloses that the protective layer is used to protect the device electronic components against oxidation and moisture (col. 4/lls. 3-8). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a protective film on the upper most layer of the semiconductor device disclosed by Greer in view of Elenius to protect its electronic components against oxidation and moisture as suggested by Kitayama.

Response to Arguments

34. Applicant's arguments with respect to claims 1-17 and 19-24 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

35. Papers related to this application may be submitted directly to Art Unit 2826 by facsimile transmission. Papers should be faxed to Art Unit 2826 via the Art Unit 2826 Fax Center located in Crystal Plaza 4, room 3C23. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2826 Fax Center number is **(703) 308-7722** or **–7724**. The Art Unit 2826 Fax Center is to be used only for papers related to Art Unit 2826 applications.

36. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Leonardo Andújar** at **(703) 308-0080** and between the hours of 9:00 AM to 6:00 PM (Eastern Standard Time) Monday through Friday (with alternated Fridays off) or by e-mail via Leonardo.Andujar@uspto.gov. If attempts to

reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn, can be reached on (703) 308-6601.

37. Any inquiry of a general nature or relating to the status of this application should be directed to the **Group 2800 Receptionist** at **(703) 305-3900.**

38. The following list is the Examiner's field of search for the present Office Action:

Field of Search	Date
U.S. Class / Subclass (es): 257/692 and 438/108	08/03
Other Documentation:	
Electronic Database(s): East (USPAT, US PGPUB, JPO, EPO, Derwent, IBM TDB)	08/03

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